BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

THE CURRENT-FEEDBACK OP AMP A HIGH-SPEED BUILDING BLOCK

By Anthony D. Wang, Burr-Brown Corp.

Although current-feedback amplifiers (CFAs) have been in use for quite some time, there is a reluctance to view them in the same light as voltage-feedback amplifiers (VFAs). For instance, the gain-bandwidth curve of VFAs has a parallel in a transimpedance-bandwidth curve for CFAs. This parameter can be used to determine the closed-loop behavior of the CFA in the same way that GBW can for the VFA. Not all the fault is with the users—the amplifier manufacturers have not standardized the CFA characterization as they have done with VFAs. This paper describes the CFA and its behavior in an intuitive manner.

HISTORICAL PERSPECTIVE

The term "operational amplifier," or "op amp" in typical engineering shorthand, has generally been associated with the transistorized voltage-feedback amplifier. It is becoming more acceptable now to include the current-feedback amplifier in the same category.

Interestingly enough, the basic architecture for the CFA might have predated the VFA although it was not until the 1980s that the CFA was itself repopularized. To appreciate the evolution of the beast, it helps to look back to some early discrete transistor circuits.

The three transistor amplifier of Figure 1 is arranged in a series-shunt configuration. However, in order to analyze the amplifier, the circuit is rearranged as shown in Figure 2.

The feedback network shows up in two places—a series network at the output and a parallel network at the emitter of the input transistor. This allows for open-loop analysis while keeping the effects of loading intact.

The loading of the output by the feedback network is generally not a problem. However, the gain of the first transistor stage is dependent on the values of the resistors in the feedback network. Thus the open-loop response will change with closed-loop gain (as the feedback network changes), which could make frequency compensation an iterative chore.

The discrete transistor circuit of Figure 3 circumvents this difficulty. Adding another transistor, Q_4, to buffer the input stage transistor, Q_1, from the feedback network illustrates this modification. This is the first step to a voltage feedback amplifier topology.

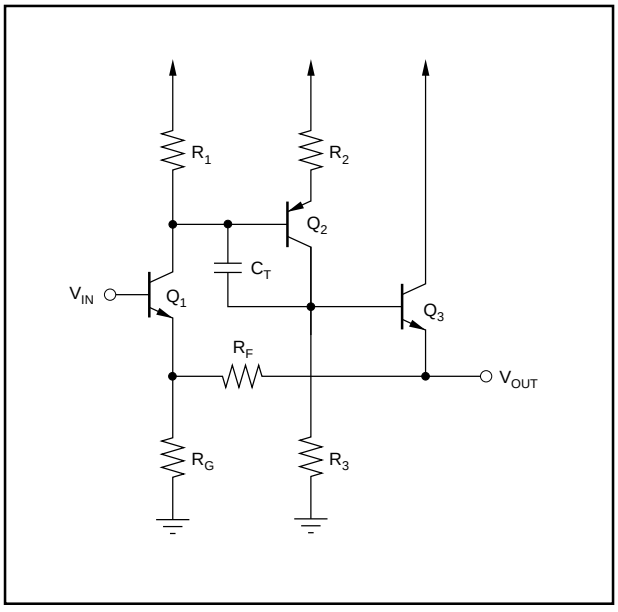

FIGURE 1. Three Transistor Amplifier.

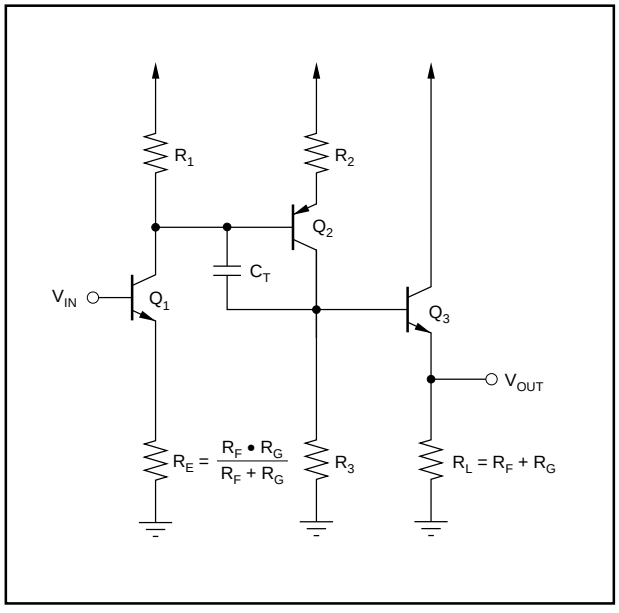

FIGURE 2. Amplifier Redrawn for Analysis.

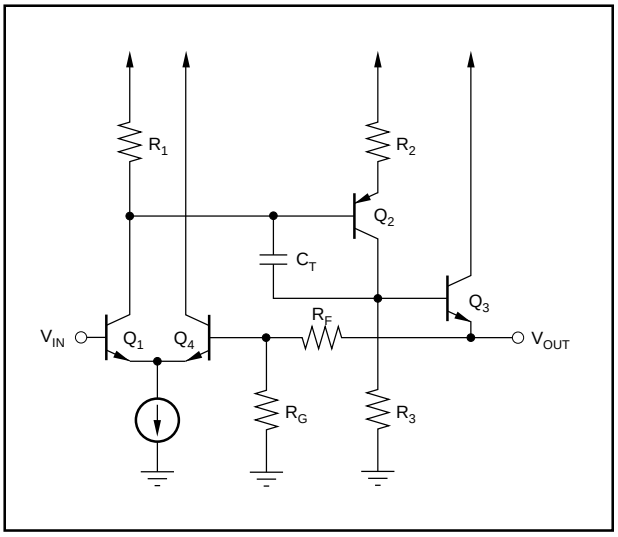

FIGURE 3. Adding a Buffer Transistor.

The added transistor presents a high impedance input to the feedback network. It also features the benefits of a balanced input, such as low offset voltage and equal input bias currents.

Of greater significance is the fact that the dynamic emitter resistance(1) of the added transistor is substituted for the parallel resistance of the feedback network in Figure 2. The first stage gain, and consequently the open-loop gain, no longer depends on the feedback network. The process of frequency compensation has one less degree of variation to be concerned with.

These two circuits illustrate the basic distinctions between current-feedback and voltage-feedback amplifiers. In both cases, the feedback network is connected to an (inverting) input node. In Figure 1, the emitter presents a low impedance input, while in Figure 3 the base presents a high impedance input.

Needless to say, the three transistor amplifier of Figure 1 can be considered the forebear for the CFA as it is known today, while Figure 3 is the template for the VFA. Figure 4 shows the same amplifier connected to a mirror-image of itself, whose transistors have been converted to the opposite polarity type. The input transistors are buffered by emitter followers for level shifting to ensure low offset voltage. This is the basis of the modern current-feedback architecture.

ANALYZING THE CFA

The study of the differential input, voltage-feedback amplifier is simplified with a technique known as "half-circuit analysis." This technique, illustrated in Figure 5, recognizes that the symmetry of the circuit presents an opportunity for simplification whereby only half the signal path needs to be considered.

NOTE: (1) The dynamic emitter resistance is tangent to the slope of the I-V curve for the base-emitter diode

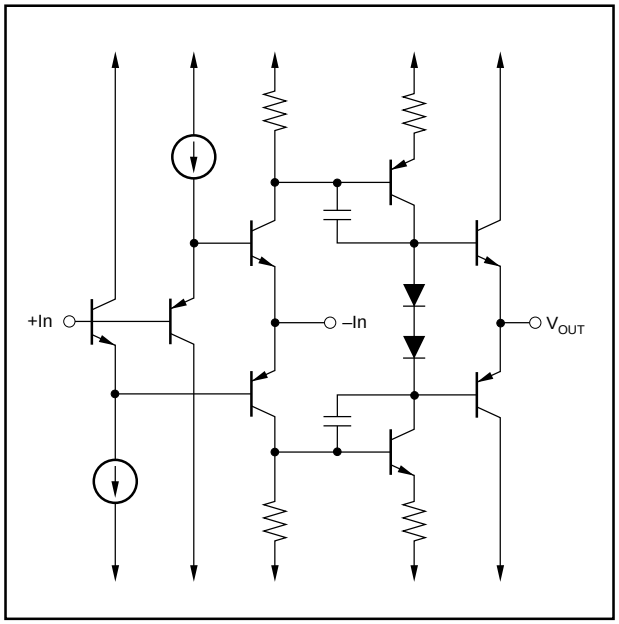

FIGURE 4. Basic CFA Topology.

The NPN current mirror of Figure 5a, which provides double-ended to single-ended conversion, still maintains balance in the circuit because the second stage output voltage is determined by the current that flows into the high impedance presented by the collectors.

Inspection of Figure 4 shows that the axis of symmetry for the CFA is centered horizontally. Therefore, the half-circuit used for analysis is the same circuit as presented in Figure 1, ignoring the input emitter follower. However, as pointed out previously, the feedback network is closely intertwined with the analysis. Therefore, the circuit of Figure 2 can be used for the analysis. The compensation capacitor, C_T, can be the intrinsic base-collector capacitor of Q_2 or an extrinsic capacitor deliberately added for compensation.

The only real difference between Figure 5b and Figure 2 is the presence of the parallel combination of the feedback network resistors in the emitter of the CFA's input transistor.

The CFA analysis is straightforward and the DC gain can be determined by inspection of Figure 2.

$$A_{VDC} = \frac{R_1}{R_E} \bullet \frac{R_3}{R_2}$$

The open-loop pole can be approximated quite accurately as the interaction of the resistor, R_1, with the Miller multiplied capacitor, C_T.

$$\omega_P \cong \frac{1}{R_1\left(\frac{R_3}{R_2} \bullet C_T\right)}$$

This analysis presumes that r_{e1}, the dynamic emitter resistance of Q_1, can be neglected ($R_E >> r_{e1}$) and that R_2 includes r_{e2}.

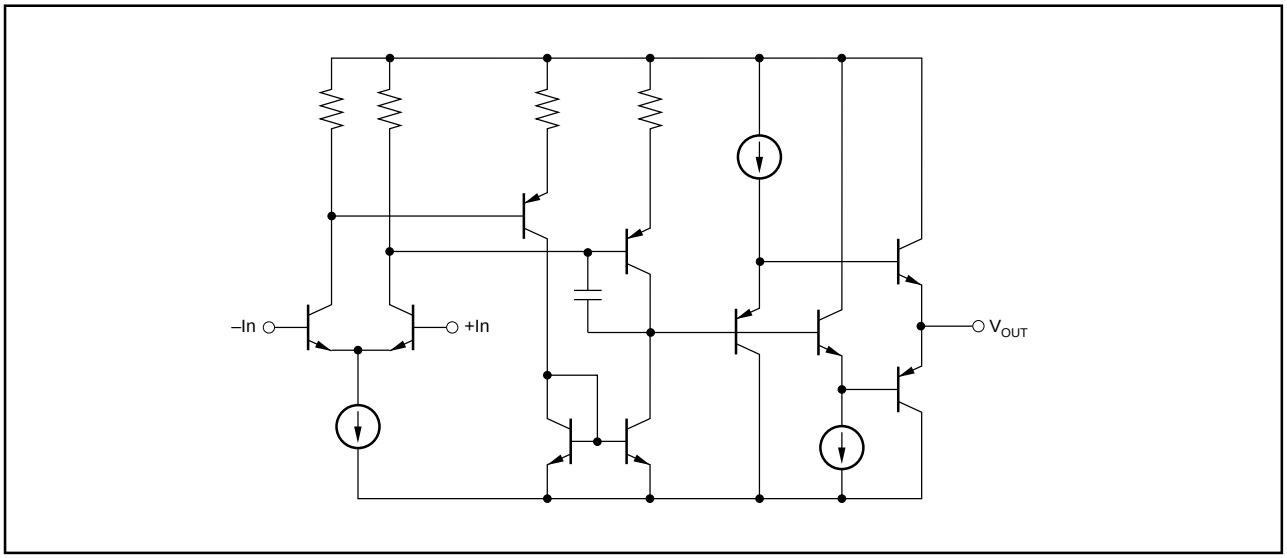

FIGURE 5a. Basic VFA Topology.

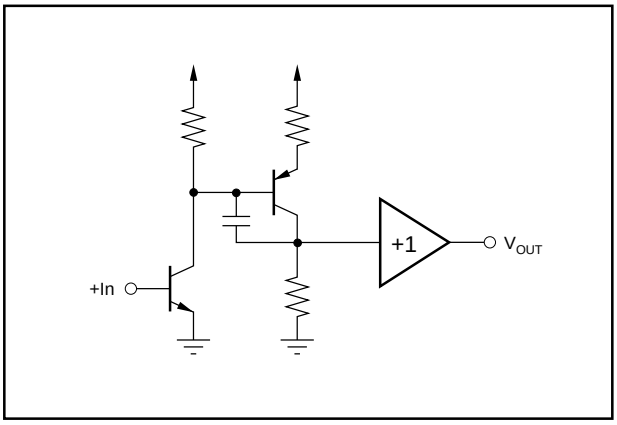

FIGURE 5b. VFA Half-Circuit.

It would be convenient at this point to define the transresistance as:

$$R_T = \frac{R_1 \bullet R_3}{R_2}$$

Note that the transresistance has the dimensions of ohms and is determined solely by elements internal to the amplifier. The previous equations can be rewritten more simply.

$$A_{VDC} = \frac{R_T}{R_E} \quad \text{and} \quad \omega_P = \frac{1}{R_T \bullet C_T}$$

Now the open-loop gain can be completely described by:

$$A_V = \frac{R_T}{R_E} \bullet \frac{1}{1 + j\frac{\omega}{\omega_P}} = \frac{R_T}{R_E} \bullet \frac{1}{1 + j\omega R_T C_T}$$

In order to arrive at this equation, it was assumed that the feedback network was known. This is the crux of the issue—the open-loop voltage gain of a CFA depends on the value of the feedback network.

Removing R_E, the feedback network term, from the equation for open-loop voltage gain yields a more general expression that describes the amplifier's open-loop performance in terms of its intrinsic characteristics. This equation would have units of ohms and would be better identified as a complex impedance, or transimpedance, Z_T:

$$Z_T = \frac{R_T}{1 + j\omega R_T C_T}$$

This is the true measure of performance for CFAs. It is now obvious why the amplifier is known as "current-feedback." The output voltage is responsive to a **current** at the low impedance inverting input node (the emitter of Q_1) that interacts with the open-loop transimpedance, Z_T.

Furthermore, the open-loop response of the amplifier is completely described by the DC transresistance, R_T, and the compensation capacitor, C_T, which is called the transcapacitance. R_T interacts with C_T to form the open-loop pole. This is graphically depicted in Figure 6.

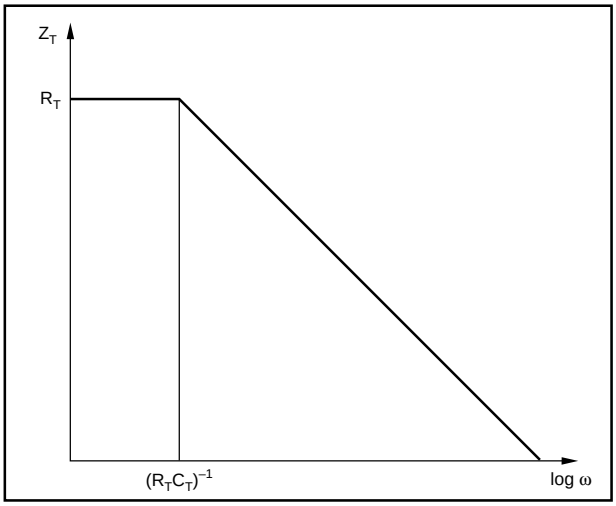

FIGURE 6. Open-Loop Transimpedance.

The ordinate axis has the dimension of ohms and is scaled logarithmically.

Having described the CFA with just two components suggests a simplified version of the half-circuit used for analysis. Figure 7 shows a convenient model that has all the essentials necessary for quick hand calculations. The inverting buffer preserves the sense of the signal as it is amplified by the Q_2 stage in Figure 2.

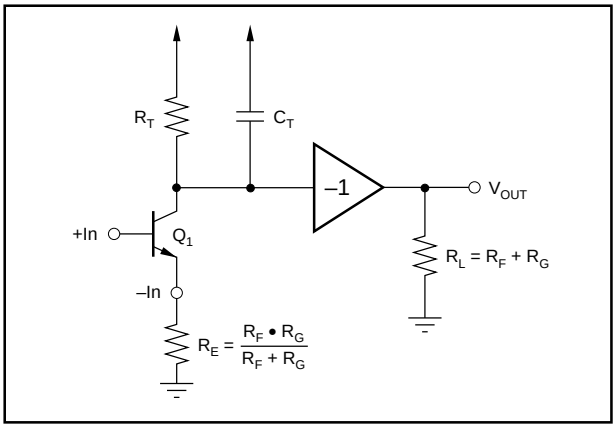

FIGURE 7. CFA Model for AC Analysis.

When determining which op amp to use for an application, comparisons with voltage-feedback amplifiers will inevitably be made. Presumably the closed-loop gain is known, which means that a feedback network can be established. Therefore, the open-loop voltage gain can be calculated for the CFA and a fair comparison with VFA can be established.

Note that the analysis described here is based on a fairly simple current-feedback topology. Although the design of integrated circuit CFAs has become more sophisticated, the open-loop transimpedance approach (Z_T) is still valid.

CLOSED-LOOP PERFORMANCE

The closed-loop response of the CFA can be described by using classical analysis:

$$A_{CL} = \frac{A_V}{1 + A_V \bullet \beta} \quad \text{where} \quad \beta = \frac{R_G}{R_F + R_G}$$

Substituting for A_V yields the following expression:

$$A_{CL} = \frac{\frac{R_T}{R_E} \bullet \frac{1}{1 + j\omega R_T C_T}}{\frac{R_T}{R_F} \bullet \frac{1 + \frac{R_F}{R_T} + j\omega R_F C_T}{1 + j\omega R_T C_T}} = \frac{\text{Open–Loop Gain}}{\text{Loop Gain}}$$

The loop gain, of course, limits the accuracy of the closed-loop gain. Note that $R_T >> R_F$ (typically R_T>100k and R_F<5k), therefore the equation can be easily simplified to:

$$A_{CL} = \frac{R_F + R_G}{R_G} \bullet \frac{1}{1 + j\omega R_F C_T}$$

The DC value of closed-loop gain is set by the feedback network, while the closed-loop pole is determined by the interaction of the transcapacitance with the feedback resistor. This latter term is what gives the CFA its much touted characteristic of gain-independent bandwidth.

A closer look at the unsimplified equation for the closed-loop gain helps to clarify this property. The DC portion of open-loop gain in the numerator is modified by the parallel combination of the feedback network, which changes with desired closed-loop gain. As long as R_F is kept constant, the loop gain expression in the denominator does not vary, nor do any of the frequency dependent terms.

Figure 8 illustrates graphically that the open-loop gain curve slides vertically to keep the closed-loop intercept frequency constant. Since R_F is kept constant, the area of the curve above the closed-loop gain stays constant.

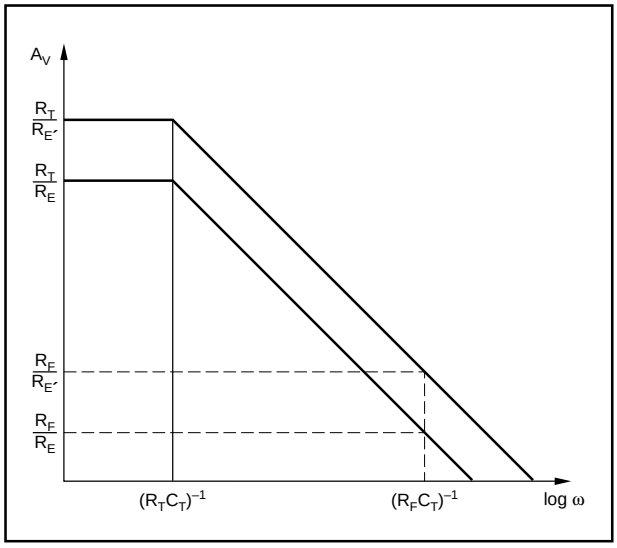

FIGURE 8. Variation of Open-Loop Gain.

The closed-loop gain expressions have been expressed as a ratio of the feedback resistor to the equivalent feedback network. This can be verified algebraically as:

$$\frac{R_F}{R_E} = \frac{R_F}{\left(\frac{R_F \bullet R_G}{R_F + R_G}\right)} = \frac{R_F + R_G}{R_G}$$

Thus, the open-loop gain varies directly with the closed-loop gain for changes in R_E as long as R_F is kept constant.

NONIDEAL CONSIDERATIONS

The assumption that the re of Q_1 can be neglected has limits. For ease of analysis, Figure 6 has been redrawn to include it as a finite input resistance, R_{IN} (Figure 9). Note that R_{IN} is internal to the CFA terminals.

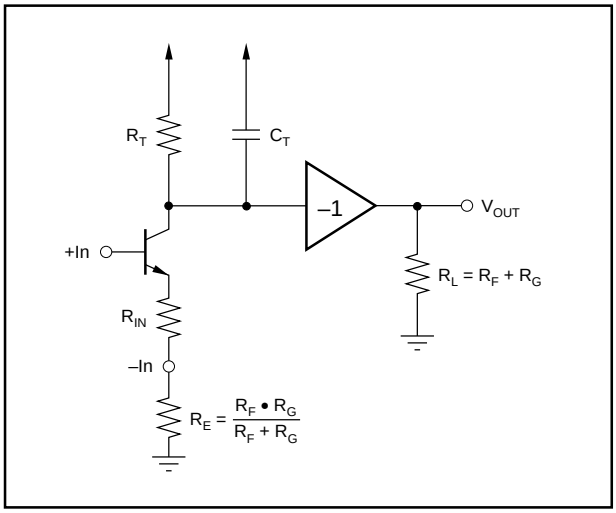

FIGURE 9. CFA Model Modified for Finite R_{IN}.

The open-loop gain equation can be modified by inspection, while a new closed-loop gain equation can again be derived using the classical approach.

$$A_V = \frac{R_T}{R_E + R_{IN}} \bullet \frac{1}{1 + j\omega R_T C_T}$$

$$A_{CL} = \frac{R_F + R_G}{R_G} \bullet \frac{1}{1 + j\omega\left(R_F + \frac{R_{IN}}{\beta}\right)C_T}$$

R_{IN} decreases the open-loop gain but not its corner frequency. On the other hand, R_{IN} does not affect the DC closed-loop gain but does modify the intercept frequency. In practice, R_{IN} includes more than just the dynamic emitter resistance—it also includes bulk resistances that are in series with the inverting input, as well as parasitic resistances external to the amplifier. Obviously, R_{IN} should be as low as possible to get the maximum benefit from a CFA.

The modified equations lead to some practical generalizations when using CFAs. The first is that the open-loop gain has a theoretical maximum and this can be conveniently estimated as:

$$A_{V(max)} \cong \frac{R_T}{R_{IN}} \bullet \frac{1}{1 + j\omega R_T C_T}$$

This is an ideal value that can never be realized since any feedback network will automatically reduce the open-loop gain. However, it is useful for estimating a CFA's merits against a particular VFA.

The second generalization is that the closed-loop bandwidth will become gain-bandwidth limited when

$$\frac{R_{IN}}{\beta} \geq R_F \Leftrightarrow R_{IN} \geq R_E$$

The latter expression makes use of the fact that the feedback factor, β, is a function of the feedback network resistors.

Once this limit has been reached, the CFA can be associated with a gain-bandwidth product, GBW.

$$GBW = \frac{1}{R_{IN} C_T}$$

The graph in Figure 10 shows an asymptotic approach to estimating a CFA's closed-loop response.

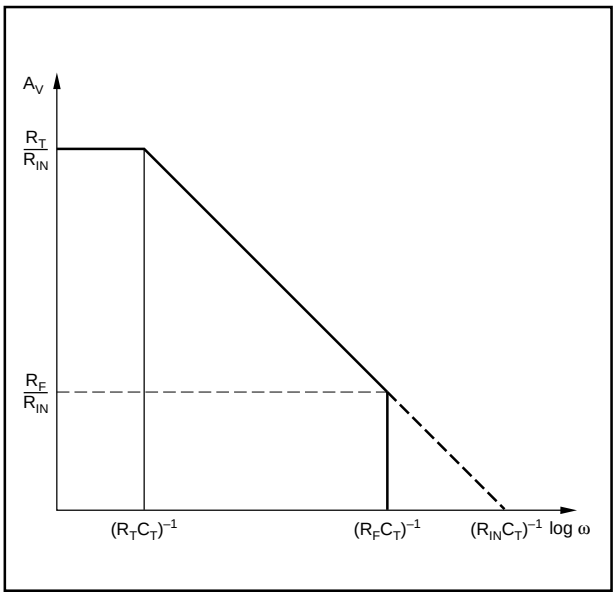

FIGURE 10. CFA Closed-Loop Performance.

To be technically accurate, it should be pointed out that the inverting input is characterized by an impedance, Z_{IN}, which does vary with frequency. Fortunately, the resistive portion, R_{IN}, dominates over most of the CFA's useful bandwidth. At high frequency, the inverting input impedance increases, which only further degrades the closed-loop performance, although the extent of the increase is generally well under an order of magnitude.

FREQUENCY COMPENSATION

The analysis so far has centered on the gain versus frequency performance without taking into account any phase shift considerations. Excess phase plagues the CFA just as it does the VFA. The open-loop transimpedance curve of Figure 6 depicts a single-pole response which would have only 90° of phase shift. Parasitic poles introduce additional phase shift to the open-loop phase response. Figure 11 displays the more complete open-loop transfer curves—both magnitude and phase.

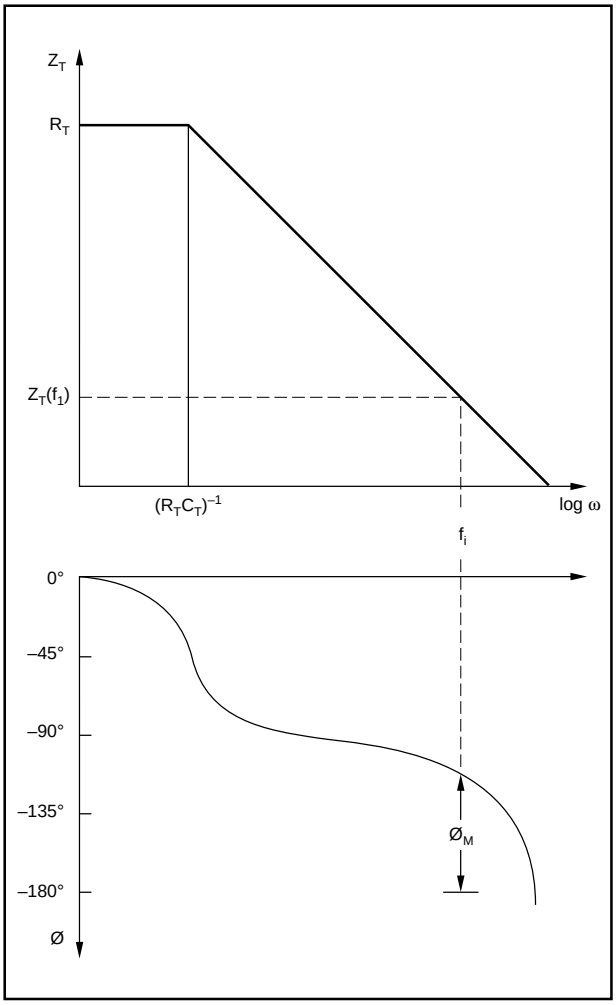

FIGURE 11. CFA Open-Loop Transfer Curves.

Since the feedback network sets the open-loop gain for the CFA, it also sets the phase margin, Φ_M. This is the crucial factor that actually determines the selection of the feedback network resistors.

The significance of phase margin would benefit from a brief review of its properties. Phase margin for operational amplifiers is measured at that frequency, f_U, where an amplifier's open-loop voltage gain has fallen to unity. It is the difference between the open-loop phase shift and –180°, where the amplifier would lose negative feedback and become unstable.

$$\Phi_M = \Phi(f_U) - (-180°)$$

The concept of phase margin is best illustrated by plotting unity gain frequency response curves as phase margin is varied (Figure 12).

As the plot shows, the optimum value for phase margin is 60°. This gives the desirable combination of broad bandwidth with flat frequency response. Note that an amplifier with 90° of phase margin, which implies a lack of excess phase, has a –3dB bandwidth less than half of the optimum response.

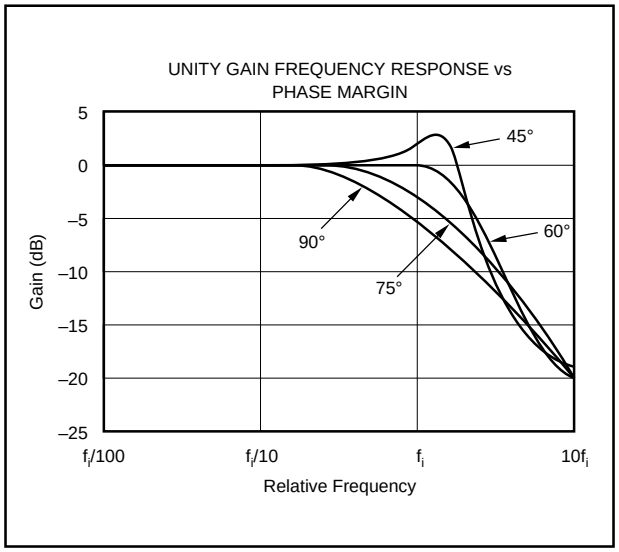

FIGURE 12. Phase Margin's Effect on Frequency Response.

A more general way of looking at this is to make the observation that the closed-loop response can be extended if the open-loop phase has fallen 120° at f_i, the frequency where the asymptote for closed-loop gain intersects the open-loop gain curve.

In VFAs, the phase margin is set by design and the user does not change it. There are a few amplifiers which allow access to the high impedance node to tailor compensation, but these are in the minority. In general, VFAs break out into two categories—compensated and decompensated.

The compensated amplifiers allow operation at unity gain but at the expense of bandwidth in higher gains. Decompensated, or undercompensated, amplifiers must be operated in gains greater than unity but have a higher gain-bandwidth product. In either case, the phase margin is predetermined.

For the CFA, phase margin is set by the user via the feedback network. However, rather than use phase margin as the design criterion, higher performance can be attained by making use of the general observations regarding phase shift and bandwidth. In other words, guarantee that the open-loop phase has fallen 120° at f_i.

The mechanics are rather straightforward because, as illustrated in Figure 8, varying the feedback network causes a simple vertical translation of the open-loop gain curve. The open-loop pole does not move and so the attendant open-loop phase shift is unaffected. The excess phase shift is also insensitive to the feedback network change. Thus, selection of a desired phase shift automatically sets the intercept frequency.

Once the intercept frequency, f_i, is determined, so is the magnitude of transimpedance, $Z_T(f_i)$. This is depicted graphically in Figure 11 by following the dashed lines up from the open-loop phase curve to the intersection with the open-loop transimpedance curve.

To realize the benefit of the –120° phase shift, the feedback network has to be selected so that the open-loop gain equals the closed-loop gain at f_i. A convenient way to visualize this problem is to concentrate on the essentials of the model in Figure 9.

The CFA model can be simplified further by ignoring the inverting buffer and focusing on that portion of the circuit which provides gain. In Figure 13 the CFA model has been reduced to an elementary transistor amplifier. The gain for this circuit is

$$|A_V| = \frac{|Z_T(f_i)|}{R_E + R_{IN}}$$

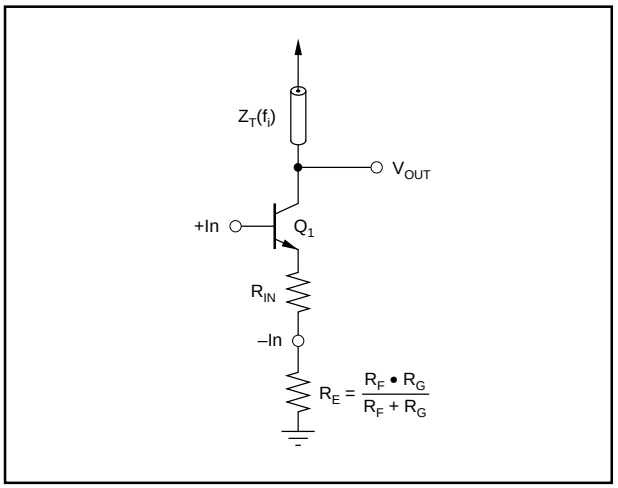

FIGURE 13. Elementary Amplifier.

The goal, therefore, is to select the necessary feedback network so that A_V equals the desired closed-loop gain. Since Z_T has previously been defined as a complex impedance, direct substitution yields a closed form solution.

$$\frac{R_F + R_T}{R_G} = \frac{|Z_T(f_i)|}{R_E + R_{IN}} = \frac{\left|\frac{R_T}{1 + j2\pi f_i R_T C_T}\right|}{R_E + R_{IN}}$$

which can be reduced to a less bulky equation:

$$R_F \cong \frac{1}{2\pi f_i C_T} - \frac{R_{IN}}{\beta}$$

Not surprisingly, this expression conforms to the plot of CFA closed-loop performance (Figure 10). For low gains, the R_{IN} term is negligible and R_F is set by f_i. As closed-loop gain increases and R_{IN}/β can no longer be neglected, R_F should be adjusted according to the equation to maintain optimum performance. When R_F approaches zero, the CFA is becoming gain-bandwidth limited and the intercept frequency must be lowered.

MODEL REPRESENTATION

The single transistor model of Figure 9 is a satisfactory vehicle to provide intuitive insight. It is by no means an accurate representation of the CFA but offers a good visual aid for the user.

A more generally accepted model for the CFA is depicted in Figure 14. This model is a very faithful rendition of the CFA from a block diagram standpoint. It can accurately account for the bipolar input and output swings that are possible with the CFA's complementary symmetry.

Comparing it to Figure 4, it is readily apparent that the unity gain buffer at the input is an accurate portrayal of the input stage between the input pins. The finite input resistance, R_{IN}, is included for completeness.

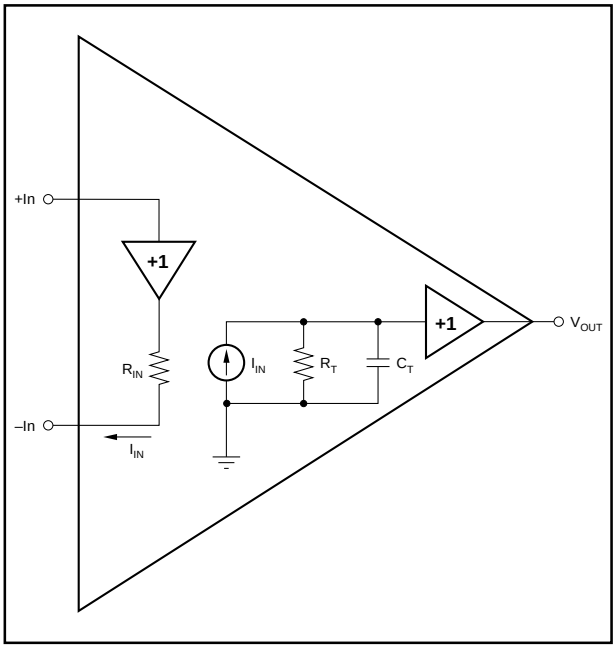

FIGURE 14. Block Diagram CFA Model.

The current-controlled current source, I_{IN}, translates the current from the inverting input to the open-loop transimpedance, again composed of R_T and C_T. The unity-gain buffer provides a low impedance source to the external load.

Either of the models is sufficient to appreciate the CFA and its performance features. Figure 9 bears a strong resemblance to the ancestral antecedent of the CFA while the latter is more readily adaptable to generating a SPICE macromodel.

Other properties of the CFA are apparent when studying these models. The slew rate is limited by the current available to charge the transcapacitance. Decreasing (R_{IN} + R_E) will certainly benefit slew performance. Minimizing C_T will increase slew rate as well as the small-signal performance.

Potential for trouble exists when parasitic capacitance is present at the inverting input. This parasitic capacitance can be the result of poor layout techniques, inappropriate use of a socket or even the wrong package. If C_p is the lumped parasitic capacitor, the open-loop gain will become:

$$A_V = \frac{R_T}{R_E + R_{IN}} \bullet \frac{1 + j\omega R_E C_P}{(1 + j\omega R_T C_T)\left(1 + j\omega \frac{R_E \bullet R_{IN}}{R_E + R_{IN}} C_P\right)}$$

This expression has added a zero and a pole to the transfer function. The zero will always occur before the pole and can be the source of trouble in some cases. If instability arises because of C_p, move the **closed-loop** pole to a lower frequency by adjusting the feedback network.

To model excess phase, the addition of a delay line can be more expedient than trying to add multiple poles and zeroes to the open-loop transimpedance. The modified transfer function is still quite compact.

$$Z_T = \frac{R_T}{1 + j\omega R_T C_T} \bullet e^{-j\omega T_D}$$

The exponential adds phase shift without affecting magnitude. A reasonable technique is to use the phase shift at the highest intercept frequency the circuit is expected to encounter.

$$T_D = \frac{1}{2\pi f_i \bullet \frac{\Phi(f_i) - 90°}{360°}}$$

Here, subtracting 90° from the open-loop phase, $\Phi(f_i)$, removes the phase shift due to the open-loop pole.

DATA SHEET SPECIFICATIONS

The open-loop transimpedance terms, R_T and C_T, and the input resistance, R_{IN}, have already been identified as necessary features to describe a CFA. Additionally, the open-loop transimpedance and phase versus frequency curves should be provided as well.

The block diagram presentation of Figure 14 suggests the other specifications that should not be overlooked. The presence of a buffer between the noninverting and inverting inputs of the CFA guarantees that the input characteristics will not match. This is the main difference between the VFA and the CFA data sheets.

The VFA data sheet typically specifies the power supply and common-mode rejection for the offset voltage only. The input bias currents are also subject to disturbances from these sources but good VFA design encourages matching impedances at the inputs to mask the effects.

The CFA does not have the privilege of bias current match, so the same effects that are specified for the offset voltage need to be measured for the two input currents. In particular, the inverting input, which is the true signal input is often the biggest source of error. It is not uncommon to see a CFA constrained to operate in an inverting gain configuration to circumvent common-mode effects.

It is not very common practice to specify power supply rejection for each supply separately but, for the CFA, it is essential. The complementary devices, NPN and PNP, should not be expected to match each other closely and usually the PNPs are the weaker. PSR measured with tracking supplies typically tend to partially cancel the errors. Real world applications usually rely on independent positive and negative voltage regulators.

The table below is for a medium performance CFA and exemplifies the amount of detail that should be provided.

PARAMETER	TYP	UNIT
INPUT OFFSET VOLTAGE		
Initial	5	mV
vs Temperature	8	µV/°C
vs Common-mode	60	dB
vs Supply (Tracking)	85	dB
vs Supply (Non-tracking)	60	dB
+INPUT BIAS CURRENT		
Initial	5	µA
vs Temperature	30	nA/°C
vs Common-mode	200	nA/V
vs Supply (Tracking)	50	nA/V
vs Supply (Non-tracking)	150	nA/V
–INPUT BIAS CURRENT		
Initial	25	µA
vs Temperature	300	nA/°C
vs Common-mode	200	nA/V
vs Supply (Tracking)	300	nA/V
vs Supply (Non-tracking)	1500	nA/V
INPUT IMPEDANCE		
+Input	5M || 2	Ω || pF
–Input	30 || 2	Ω || pF
OPEN-LOOP TRANSIMPEDANCE		
Transresistance	440	kΩ
Transcapacitance	1.8	pF
OUTPUT CHARACTERISTICS		
Voltage	12	V
Current	150	mA
Output resistance, Open-loop	70	Ω

TABLE I. Source: BB OPA603 Data Sheet.

SPICE SIMULATION

The combination of declining hardware costs with increasing computing horsepower has made circuit simulation a required part of the design cycle. This has forced the op amp vendors to supply the macromodels for their product offerings.

These simulation tools have been offered in varying degrees of complexity, from the simple Boyle model to simplified circuit models, which utilize full transistor models in the signal path. There has been a growing consensus that this latter approach is necessary for the high bandwidth amplifiers.

There can be no doubt that having these models available helps to fill in the gaps from incomplete data sheets. Although the models may not necessarily be configured for worst case process extremes, there may be some performance peculiarities that can be discovered through their use. The pitfall to be aware of is that even the simplified circuit models generally idealize the biasing circuitry, which may mask some second order PSR and CMR effects.

Figure 15 shows two alternative simulation schemes. In Figure 15a, the CFA is driven open-loop to measure the open-loop transimpedance and input resistance. This requires two separate simulations. The first uses a voltage-controlled current source to find the dc value of inverting input current to servo the output to zero. The second pass is the ac simulation to actually measure the transimpedance.

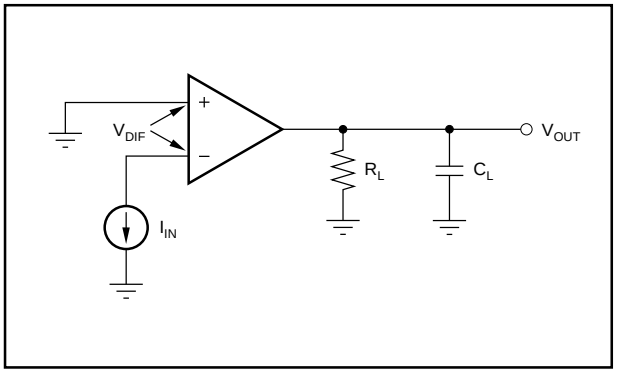

FIGURE 15a. Open-Loop Simulation.

Figure 15b uses a zero volt battery to measure the inverting input current while the op amp is in a closed-loop configuration. This measures an effective transimpedance that includes the common-mode effect.

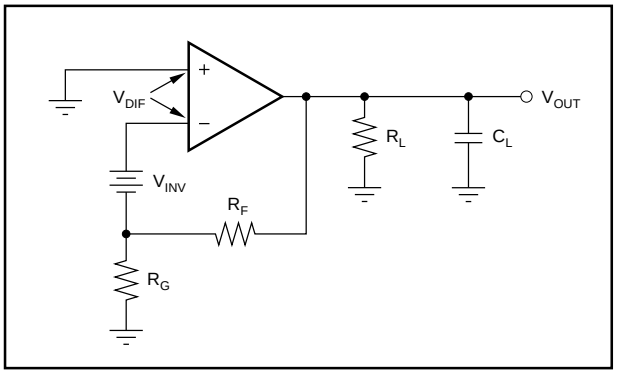

FIGURE 15b. In Circuit Measurement.

The circuit of Figure 15a was simulated with the following listing:

```
* CURRENT-FEEDBACK OPEN-LOOP SIMULATION *
* file: CFA-OL.CIR
***** Simulation Commands *****
.options noecho nomod numdgt=8
.op
.ac dec 20 10 200meg
.probe
***** Library Files *****
.lib burr_brn.lib
***** Circuit Listing *****
vp 7 0 15
vm 4 0 -15
*ginv 2 0 6 0 -1
inv 2 0 dc -38.3pa ac 1
x603 0 2 7 4 6 opa603
rl 6 0 100k
.end
```

Figure 16a is the plot of input resistance as measured by dividing the ac voltage by the ac current. Note that for the useful frequency range of the amplifier (roughly 100MHz), R_{IN} varies less than 10Ω. The open-loop transimpedance is displayed in Figure 16b. Here the magnitude has fallen from a DC value of 790kΩ to 1.5kΩ at 51.6MHz, which is where the open-loop phase has fallen to –120°.

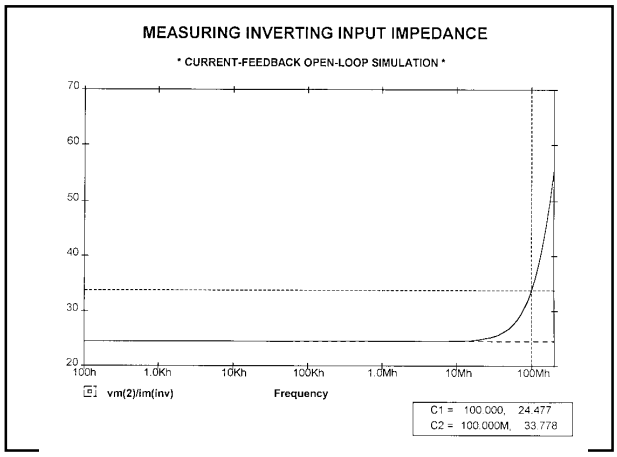

FIGURE 16a. Measuring the Inverting Input Impedance.

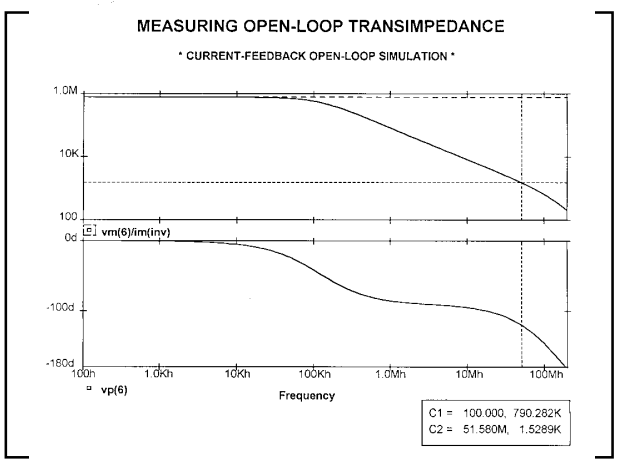

FIGURE 16b. Measuring Open-Loop Transimpedance.

The circuit of Figure 15b was simulated with the following listing:

```
* CURRENT-FEEDBACK CLOSED-LOOP SIMULATION *
* file: CFA-CL.CIR
***** Simulation Commands *****
.options noecho nomod
.ac dec 20 1000 200meg
.probe
***** Library Files *****
.lib burr_brn.lib
***** Circuit Listing *****
vp 7 0 15
vm 4 0 -15
vin 3 0 dc 0 ac 1
x603 3 inv 7 4 6 opa603
vinv inv 2 dc 0
rf 6 2 1450
rg 2 0 1450
.end
```

The plot in Figure 17 shows the intersection of the open-loop gain curve with the closed-loop gain asymptote which occurs at 45.7MHz. The open-loop phase has the value of –120° at this frequency and the broadbanding of the closed-loop gain is quite evident. Note the technique used to generate the open-loop gain curve.

The equation relies on the calculation of open-loop transimpedance (via the current in the battery) which is divided by the sum of the equivalent feedback network plus the input resistance.

$$|A_V| = \frac{|Z_T(f_i)|}{R_E + R_{IN}} = \frac{\frac{vm(output)}{im(battery)}}{R_E + R_{IN}}$$

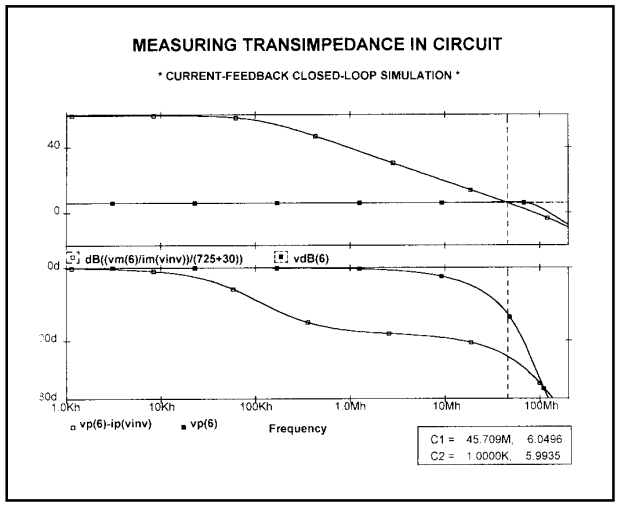

FIGURE 17. Slope Intercept Curves for CFA Circuit.

MEASUREMENT CIRCUITS

If companies could ship only simulation files to their customers, life would be so easy. Sooner or later, a reality check has to be made. The following circuits have been proven to be quite reliable for measuring the CFA performance parameters.

The low impedance of the inverting input node presents a special problem for the test engineer. Conventional op amp test circuits cannot easily separate the individual parameter variations. The most logical solution is to test the CFA with a current mode test circuit.

Figure 18 shows the basic current pump topology used in the DC test circuit. It consists of a JFET input op amp, a P-channel MOSFET and a unique current reference circuit which includes two very accurate current sources and a high precision current mirror.

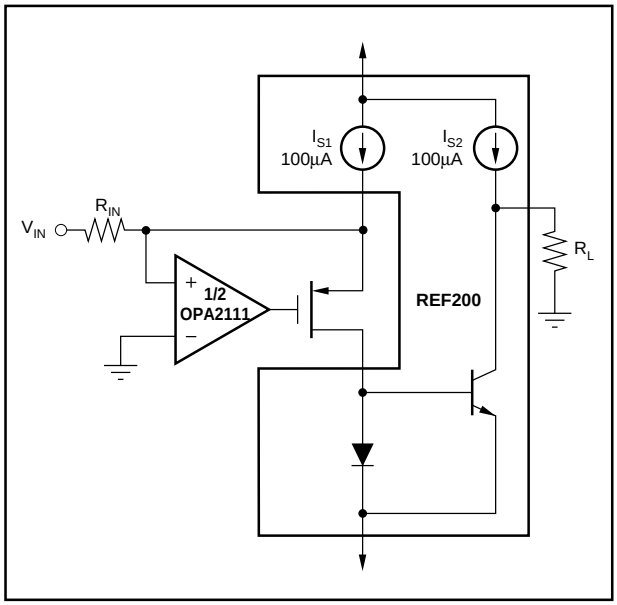

FIGURE 18. Current Pump Topology.

The high gain of the JFET input op amp (VFA) constrains its inverting input to stay at null ground by controlling the current flowing through the MOSFET. If V_{IN} is positive, a current equal to V_{IN}/R_{IN} is shunted to the current mirror input. If V_{IN} is negative, a matching V_{IN}/R_{IN} is provided by the 100µA current source, I_{S1}, and the input to the current mirror decreases. This is an inverting current pump, a positive voltage causes the output to sink current and a negative input causes the output to source current.

The full test circuit is shown in Figure 20. The input offset voltage of the DUT is measured directly by the instrumentation amplifier, A_1. The RC filters minimize noise and protect the inputs of A_1 from overload transients.

Amplifier A_2 maintains the common-mode bias by forcing the current pump (A_3, M_1, IC_1) to keep the noninverting input of the DUT equal to the input, V_{CM}. The output of A_2 driving the 100kΩ input resistor to the current pump is a measure of $+I_b$.

Amplifier A_4 constrains the DUT output to be the negative of the input voltage, V_f, by forcing the current pump (A_5, M_2, IC_2) to drive the low impedance inverting input. The amount of inverting current drive is reflected by the output of A_4.

All DC parameters, including R_T and R_{IN}, can be measured independently and directly. When adapted to a measurement card for the HP Semiconductor Analyzer, the test parameters can be displayed as slopes to determine the limits of linearity.

Figure 19 details an open-loop transimpedance test circuit which, when mated with a network analyzer, will provide the open-loop frequency response curves.

The input ladder network divides the input by 20,000 to provide a low current level signal to the inverting input of the DUT. The 500Ω value for the input resistor dominates the small but finite input resistance of the CFA. The A_1 integrator servos the output to zero by sensing the DUT output and feeding a small current back to the input. A_2 buffers the DUT output and drives the 50Ω input of the network analyzer.

The only caveat is to take into account the gain and phase rolloff of A_2. Automated network analyzers allow for compensation by storing an "offset" sweep which is subtracted from the actual signal sweep.

Although the network analyzer will scale the output in dB, the transimpedance can be determined by using the following equation:

$$Z_T = 500 \bullet \log^{-1}\left(\frac{\text{dB magnitude}}{20}\right)$$

The transcapacitance can be found by extrapolating the open-loop pole.

CONCLUSION

CFAs are not difficult to comprehend and work with if the basic relationships between R_T, C_T, R_{IN} and open-loop phase are kept in mind. The lack of balanced input nodes require extra care be taken with applications requiring DC accuracy. Simulation is a wonderful tool for the early design stages but only actual measurements will grant peace of mind.

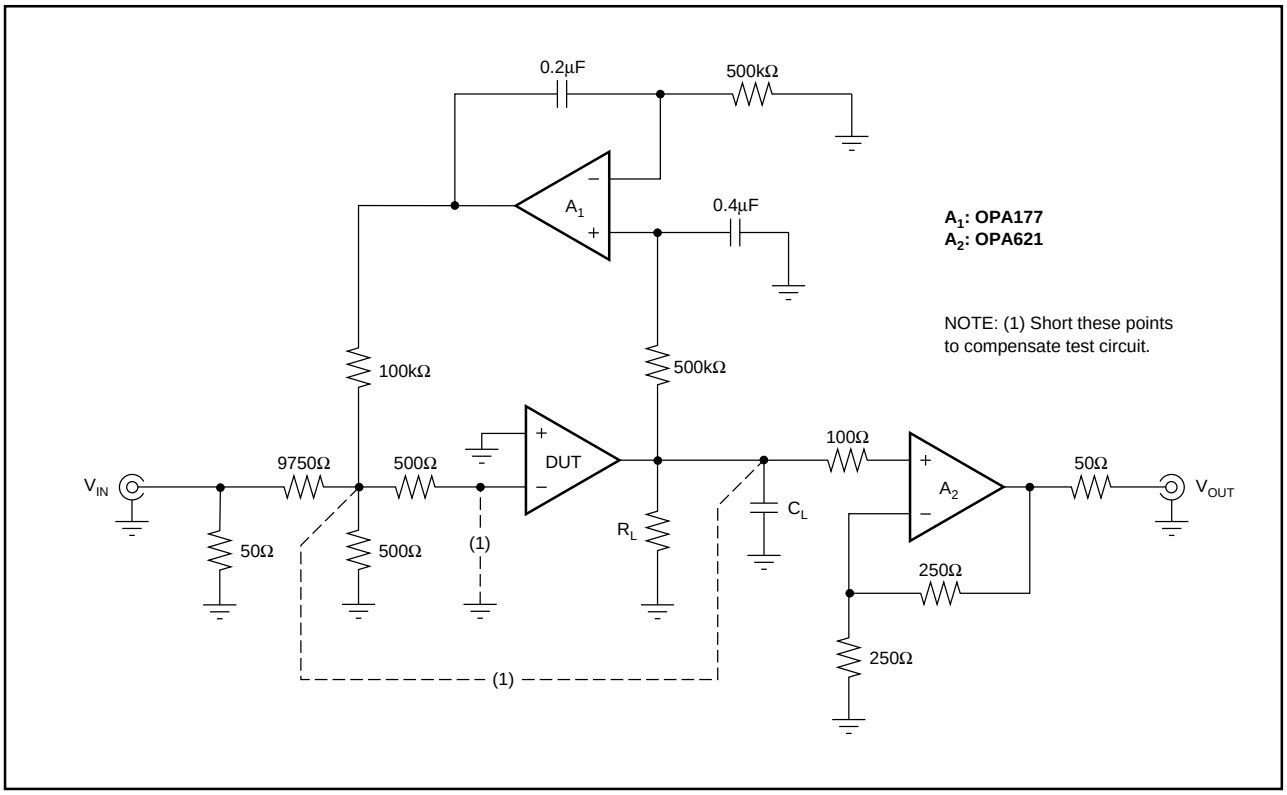

FIGURE 19. Open-Loop Frequency Response Test Circuit.

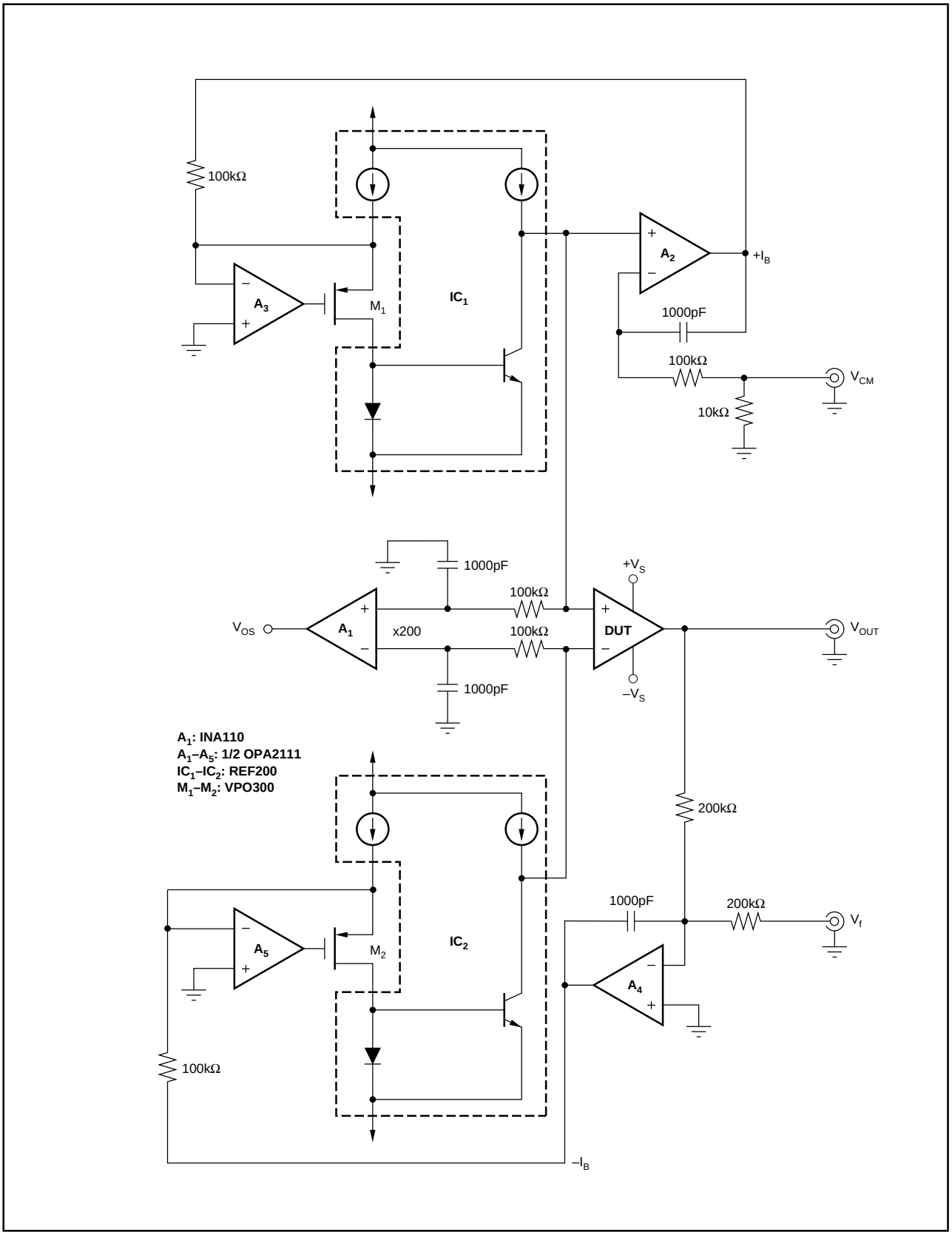

FIGURE 20. Current Mode CFA Test Circuit.